D3.3 - Performance and reliability figure of merit definition

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1 Introduction

The consortium of BeforeHand aims at developing phase change materials (PCM) targeted to address key applications in the automotive sector, secure market and general purpose microcontrollers. In particular, the automotive market is very demanding in terms of reliability.

The technology requirements for automotive microcontroller units have been shown in MS.1 and are reported in Table 1 for convenience.

Product	Technology
Direct code execution, access time < 10… 20ns	High reading current of code memory (>20µA typ)
Frequent updates of data memory (e.g. start/stop systems)	Data Memory w/ high endurance & retention lifetime (500kcycles + full operating lifetime)
Under hood applications (e.g. engine & gear shift control)	Broad temperature range (T_j = -40…175C)
Safety critical applications	Ultra-low failure rates <1ppm

Table 1

The BeforeHand consortium will address both the broad temperature range requirement, necessary for automotive applications, as well as the requirements in terms of endurance and retention, as derived from memory technology.

To address all these objectives, the approach of materials engineering will be adopted, with the realization of single cell memory devices capable to test new materials and/or novel heterostructures. The selected materials should be able to guarantee the realization of test vehicle devices which exhibit a decrease of programming current, an improved data retention and a lower temperature induced resistance drift, compared to the non-volatile memory target for automotive. Table 2, here reported from MS1, shows the expected targets.

The figures of merit of the PCM "heterostructures" grown in the consortium and of the developed test vehicle devices are defined to fulfil these requirements. The reliability aspects, such as thermal stability, cyclability and resistance drift are also considered.

In this report the methodology that will be adopted to evaluate the performance and reliability of both materials and single cell devices is presented. First, we set specific criteria on relevant figure of merits to be able to screen promising materials and heterostructures. Such promising materials will be deposited in the cell devices. Second, the electrical evaluation of the single cell will be used to decide on the best material/heterostructure that will be used to fabricate the demonstrator in WP5.

Feature	NVM Target for automotive MCU	BeforeHand target – single cells
Write speed	< 2ms	< 2ms
Cell size	< $50F^2$	< $50F^2$
Programming energy	< 150pJ	< 150pJ
Programming window	> 50X	> 50X
Programming current	-	30% decrease over Ge-rich GST
Set drift@ 150°C	-	< 2X Rset
Endurance	$5 \cdot 10^5$	> $5 \cdot 10^5$cycles
Data retention	>20y	>20y
T max	165C	165C
Soldering compliance	Yes	Yes
Film Thermal stability	Compatible w BEOL process	Reduced material segregation / intermixing vs Ge rich GST

Table 2

2 Figure of merit definition and performance evaluation of thin films

One of the main challenges for the employment of PCM technology in automotive applications is the high operating temperature. Automotive specifications for data retention are 1 hour at 240°C for both SET and RESET, and 2 hours at 230°C (JEDEC standard protocol for reflow soldering-like profile validation) [1]. In applications such as smartcards and security, for which the integrity code must be preserved, the memory must retain the information after the soldering flow. This means, according to the JEDEC standard reflow profile, that the information must be preserved at a peak temperature of 260°C for more than 30 s.

It has been already shown that materials engineering is a clear path to improve the high temperature stability. In particular, ST demonstrated that Ge-rich $Ge_2Sb_2Te_5$ alloys (Ge-rich GST) can be successfully employed to make PCM devices with retention capability > 10 years at 150°C, enabling PCM for embedded automotive applications [2,3]. For this reason, Ge-rich GST material will be employed as a material reference for benchmarking BeforeHand materials.

Within the BeforeHand project, the realization of processing/storage devices will be achieved through the development of new materials combination.

The selected materials for the integration in the test vehicle will be both composite materials, such as Ge-rich GST, and multilayers with different compositions.

The main figure of merit for the thin films evaluation is, therefore, the **crystallization temperature**.

2.1 Figure of merit: crystallization temperature

In order to determine the crystallization temperature, thin amorphous films with different stoichiometries, prepared by the partners of the consortium, will be characterized by **isochronal anneals**. The conversion of the amorphous film into the crystalline phase will be followed by **electrical measurements**, using four point probe configuration, and/or by in situ **reflectivity measurements**. The optical measurements will be employed for those stoichiometries in which the electrical resistance contrast between the amorphous and crystalline phase is also associated with an optical contrast. This is the case of several materials that will be studied in the project, such as Ge-rich GST alloys, GeTe, GaSb. In particular, the reflectivity change upon crystallization is a powerful technique to study the crystallization process in all the situations in which the resistivity cannot be easily measured, such as, for example, in presence of a thick insulating capping layer or for phase change films deposited on conductive materials, such as the silicon substrate or the heater (typically TiN). Nevertheless, all these situations deserve a careful evaluation, since interfaces with different materials are present in a real memory cell and some of them are crucial for the device operation. In the case of heterostructures made by a stack of layers with different compositions, the two films will be first separately studied, determining the crystallization temperature of each composition, and then the stack will be investigated.

Isochronal anneals of 3 minutes with increasing temperature up to 300°C will be performed. The crystallization temperature will be determined as the temperature at which the first derivative of the resistance (or reflectivity) versus temperature exhibits a maximum.

A material (or a stack of materials) grown within the consortium will be considered relevant for device realization when it exhibits crystallization temperature > 200°C under 3 min isochronal anneals, as previously defined.

2.2 Figure of merit: resistance contrast

The other important figure of merit that will be taken into account for materials selection is the **resistance contrast** between the amorphous and the crystalline phase, which is required to be at least 1 order of magnitude, even at high temperature (150°C). This can be evaluated by sheet resistance measurements of the two phase as a function of temperature.

The employment of phase change materials with different compositions, each one with its own peculiar electrical, optical and thermal properties, both in the amorphous as well as in the crystalline phase, however requires the adoption of proper models to describe and predict the behaviour of the composite material.

In the project we intend to use approaches based on the effective medium approximation, developed by Bruggeman [4], to describe the optical and electrical properties of layers with two coexistent phase change materials and / or with crystalline and amorphous regions during phase change. As an example, Bruggeman [4] describes how to calculate the electrical conductivity σ and the dielectric function ε for various shapes of composite materials as function of the "dopant" (σ_d and ε_d) and the host material properties (σ_0 and ε_0).

In the case in which there are two layers of different materials, such as, for example GaSb and Sb_2Te_3, oriented parallel to the direction of the electrical current, the effective dielectric function is a function of the volume fraction of the "dopant" phase f, and it is given by:

$\varepsilon_{eff} = (1-f)\,\varepsilon_0 + f\,\varepsilon_d$

The electrical conductivity is: $\sigma_{eff} = \sigma_0 + f\,(\sigma_d - \sigma_0)$

In the case, instead, of materials made by spherical clusters embedded in a matrix with different composition, such as for Ge-rich GST, in which part of the excess Ge is expected to form spherical pure Ge grains, the dielectric function according to Bruggeman is:

$\varepsilon_{eff} = 1/4[\,2\varepsilon_p - \varepsilon'_p + \sqrt{\,[(2\varepsilon_p - \varepsilon'_p)^2 + 8\,\varepsilon_0\,\varepsilon_d]}$

With $\varepsilon_p = (1-f)\varepsilon_0 + f\,\varepsilon_d$ and $\varepsilon'_p = f\varepsilon_0 + (1-f)\,\varepsilon_d$

The same equations are also valid to describe the crystallization process, in which the "dopant" is the crystalline phase into the hosting amorphous matrix [5].

This theoretical approach can be also employed to design heterostructures for which an optimised resistance contrast is expected. In the project three different approaches will be followed for the device realization: the vertical cell (SCV), the line cell (LSC) and the nanowires. By adopting a SCV or LSC device, the direction of the electrical current is opposite, compared to the direction of growth of the layers. It is therefore crucial to understand in which condition a given heterostructure is more promising for an optimised design and modelization, as shown in Fig. 1.

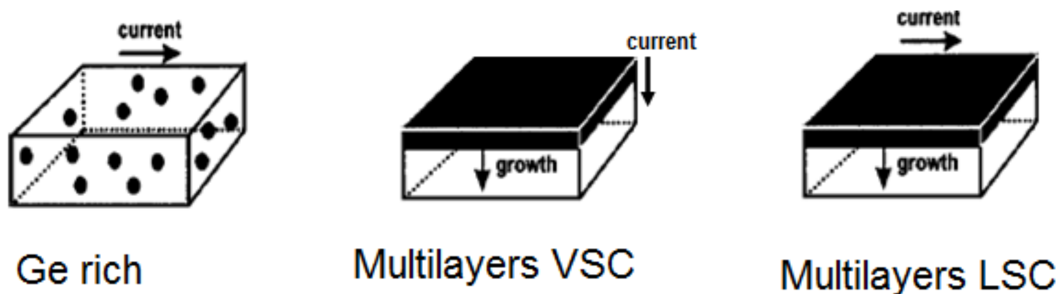

Fig. 1: Direction of the electrical current in different materials studied in the project and for different devices.

3 Figure of merit definition and performance evaluation of test vehicle device

Single cell devices will be manufactured in the crystalline state, since typically after manufacturing, the material is in the crystalline phase, because of the thermal budget of the back end of line (BEOL) processes. Therefore the first test of the pristine device will be the RESET process, to convert the crystalline film into the amorphous phase.

3.1 Measurement procedure

To perform a full characterization of the PCM cell we will:

1. apply voltage pulses with rise/fall time on the order of few ns, to perform RESET/SET operation
2. detect the current I flowing during the programming pulses, by measuring the current voltage (I-V) characteristics

3. perform a precise measure of the device resistance R, by collecting the (R-I) programming curves

For the RESET process we will use a sequence of pulses with increasing voltage from a minimum value V_{min} to a maximum value V_{max}, as shown in Figure 2. The width of each pulse will be 300 ns, with typical rise and fall time of 10 ns. The resistance is measured between one voltage pulse and the subsequent. The programming current is measured during the pulse. The V_{max} value is increased of a step ΔV at each iteration, until a RESET condition is reached. The RESET condition is defined as the achievement of a fixed RESET resistance value or of a resistance saturation.

After the first RESET, the cell is reversed back into the SET state, i.e. in the crystalline structure by adopting a staircase down, consisting in a sequence of pulses with decreasing intensity from V_{res} to 0 V, and constant width (300 ns).

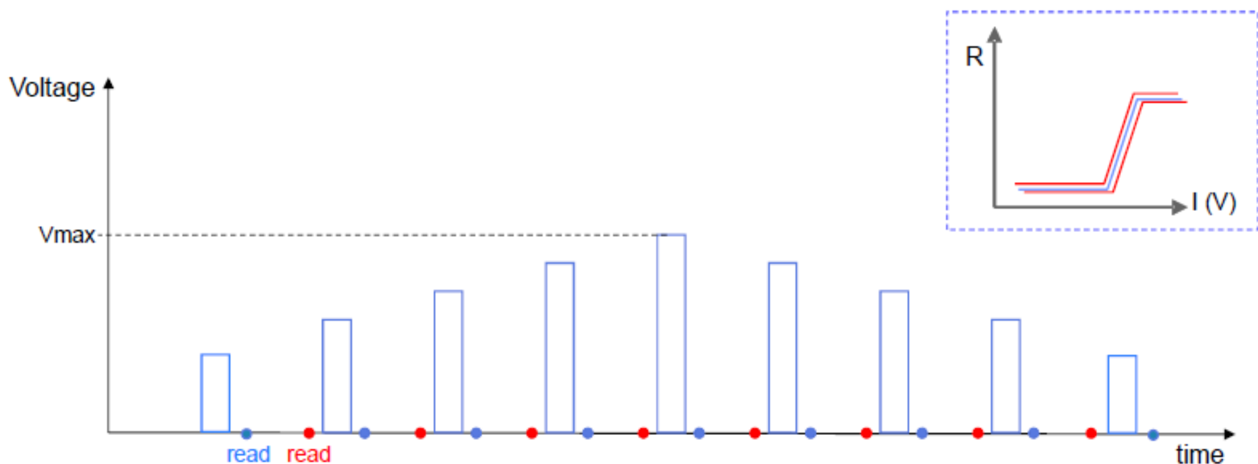

Figure 2: Staircase sequence with increasing voltage for the RESET process, and decreasing voltage for the SET process. The inset shows the programming curve R-I

Once the RESET conditions have been identified, it is possible to evaluate the SET window by performing a pulse sequence as shown in Figure 3, in which each pulse of an increasing staircase sequence is followed by a pulse V_{res}, (RESET to RESET).

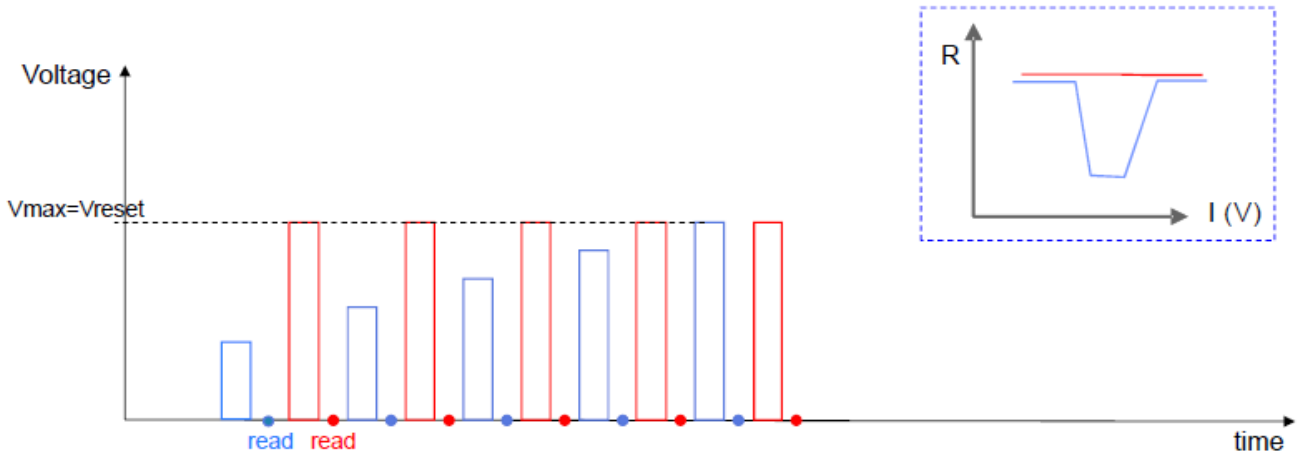

Figure 3: Voltage pulse sequence to evaluate the SET window (inset).

3.2 Figure of merit: programming current and RESET Voltage

The two main figures of merit in device programming are the programming current I_p and V_{res}. Considering as a benchmark the devices with Ge rich GST225 devices, for the new heterostructures grown in the project, a reduction of 30% of the programming current is expected. The complete testing sequence is reported in Table 3.

label	sequence	Start / End	meaning
U	Up	Pristine to RESET	Initialization step 1/2
D	Down	RESET to SET	Initialization step 2/2
U	Up	SET to RESET	Observe the programming window and collect the programming current
U	Up	RESET to RESET	Catch Vth on I-V curve
D	Down	RESET to SET	Verify the reproducibility of program operation

Table 3

4 Reliability Figure of merit definition

Once we have realized functioning devices with new materials, we will study the reliability of such devices, starting on the material properties, and then focusing on the devices. The reliability aspects we will take into account are the retention and the endurance.

4.1 Retention

The retention is one of the crucial aspects to be taken into account for reliability evaluations. The ability to retain the same resistance value for a long time, even at high temperature, is dominated by two independent processes: the spontaneous re-crystallization of the amorphous phase and the resistance drift.

As already observed, ST has demonstrated retention capability **> 10 years at 150°C** for Ge-rich GST alloys. In order to assure the same retention with novel heterostructures, the devices in the RESET state will be tested after bakes at different temperatures. As failure criterion we take the retention time corresponding to a decrease of 33% in the RESET state initial resistance value. The retention times obtained at different temperatures are then used in an Arrhenius plot to extrapolate the 10 years. Such an extrapolation can be performed in the single cell devices, but can be also done at the thin film level, by evaluating the activation energy for crystallization upon isothermal anneals.

The other issue representing a fundamental limitation to the retention is the **resistance drift**. This is usually observed in the amorphous state (RESET), but it may also occur in the SET state, especially when different materials are placed together, since diffusion and intermixing may occur. The resistance drift has been shown to follow a power law:

$R(t) = R_0 (t/t_0)^{\nu}$

Where R_0 is the initial resistance at time t_0 and ν is a drift coefficient, which, for amorphous GST, typically has values of 0.05-0.11 [6]. In order to evaluate the drift, the resistance is measured as a function of time and at different temperatures. This study can be performed in the single cell, as well as at thin film level, both in the amorphous or crystalline state. Although there are several techniques that have been proposed to mitigate the resistance drift, such as, for example, compensation techniques at the read time, lower drift coefficient is desired in order to minimize the drift. The target value in the project for the RESET state is **ν < 0.13**.

For the drift of the SET state, the target is < 2x Rset at 150°C.

4.2 Endurance

Cycling endurance has long been one of the strengths of phase change memory, allowing 10^{10} SET-RESET cycles without significant degradation of resistance contrast. Two different failure modes have been observed to occur after cycling [7], termed as “stuck-RESET" and “stuck-SET" failure, as shown in Figure 3.

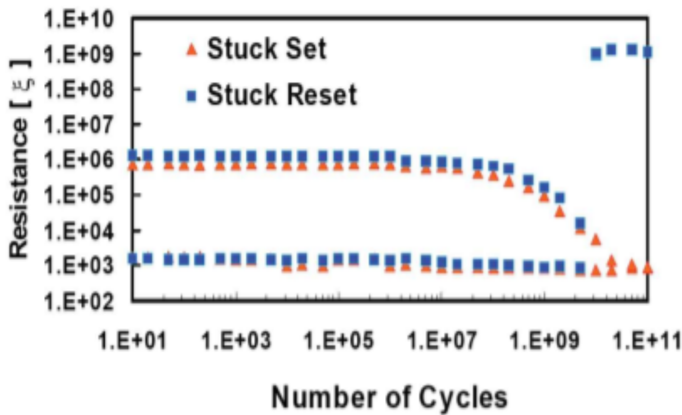

Figure 4: SET and RESET resistance during cycling, reported from Ref. [7].

In a stuck-RESET failure, the device resistance suddenly increases, reaching a value that is much more resistive than the RESET state. These failures are typically attributed to void formation or delamination, typically at a material interface such as the heater-to-GST contact. In a stuck-SET failure, a gradual degradation of resistance contrast is typically observed. The cell seems to change its characteristics so much that upon cycling, the original RESET pulse becomes less effective at creating an amorphous region in the device than before, mot likely due to a change in the composition, with a corresponding increase in the melting temperature. For the stuck SET usually the pulse duration has stronger effect than the amplitude [8]. In particular, the time-spent-melting the PCM material is a critical factor. Most of the measurements on mushroom cells built from $Ge_2Sb_2Te_5$ material [9,10] have shown atomic migration takes place upon cycling, possibly leading to performance variations over lifetime and eventually to device failure [11,12]

As a general trend, it has been shown that Ge moves away from the hottest area (GST/heater interface) towards the coldest outer boundary of the molten dome, with negligible differences between polarities. On the other hand, Sb moves towards the hot interface with, however, visible dependence on polarity. Sb pile-up at the interface higher for forward program. Finally, Te does not show a specific sensitivity to the thermal gradient, remaining almost constant in the molten volume, with a slight dependence on polarity [13]. The driving forces involved in the migration mechanisms are both electrical and thermal. It is well accepted that electromigration plays a role, as well as the thermo-electric Thomson effect, in which the overlap of temperature gradients with electrical current can lead to additional heat generation or absorption.

In the particular case of Ge-rich GST, it has been shown that during the initial seasoning procedure, Ge segregates at the periphery of the liquid zone [14], impoverishing the melted

volume. Such a stoichiometry modification seems to occur only during the initialization process, leading then to a stable active cell. It has been shown that the Ge segregation outside of the liquid volume is essentially due to the high Ge diffusion coefficient in the melted material (on the order of 10^{-5} cm^2/s) [15], and occurs even in the absence of applied electric field.

Therefore atomic diffusion, with the subsequent stoichiometry variation, may be a factor playing a relevant role in the endurance, especially when the device is made by two different compositions and operates at high temperature. In order to investigate the material stability upon cycling, endurance experiments, in which the device is stressed by several electrically induced programming events, will be correlated with HR-TEM physical analysis in order to clarify possible intermixing of the layers of the heterostructures or compositional variations.

The target endurance for the devices is **> $5x10^5$ cycles**.

5 Conclusions

In this deliverable we have defined the figure of merit and the testing procedure for the performance evaluation of: (a) thin film heterostructures, (b) single cell devices, (c) reliability.

The material and device characterization for the performance evaluation will follow the flow chart shown in Figure 5.

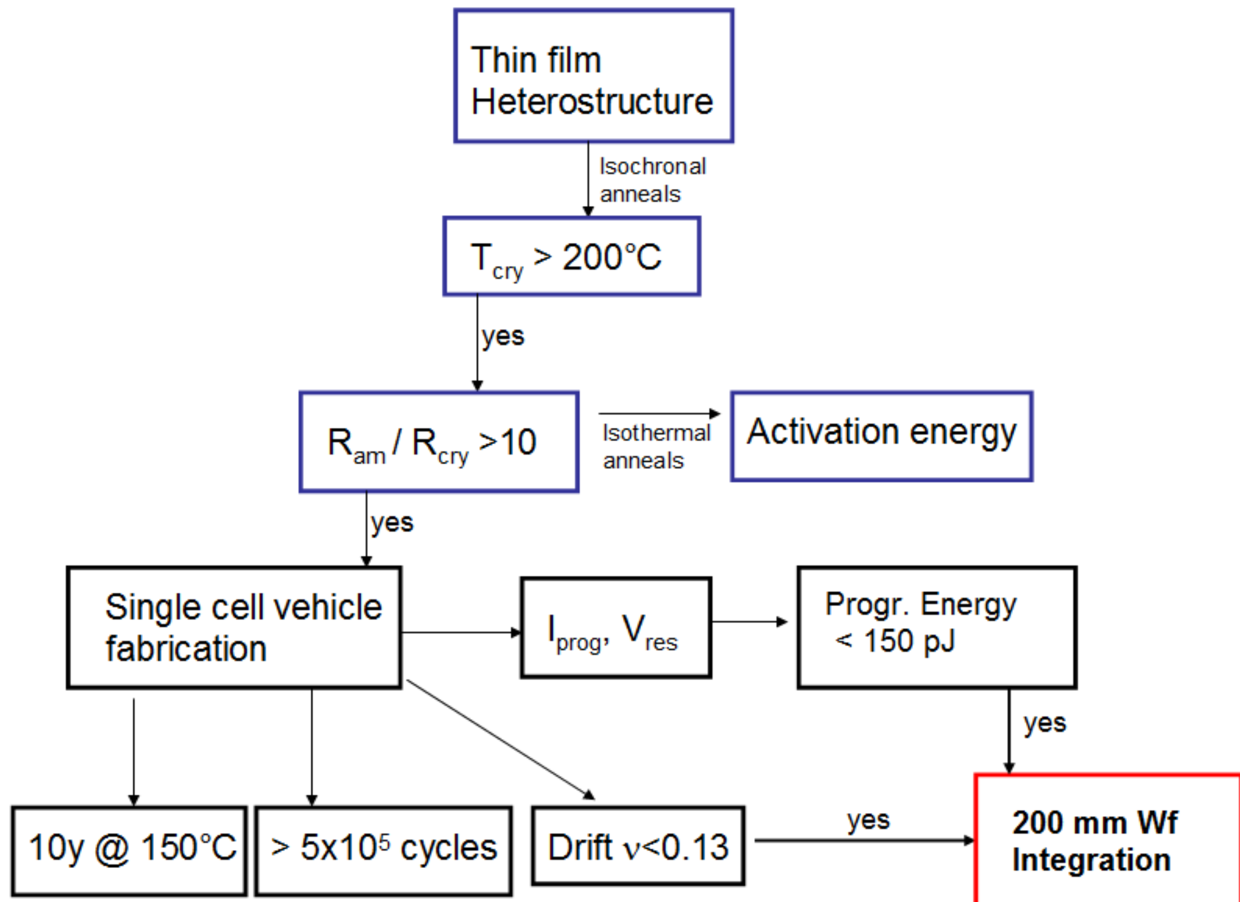

Figure 5: Performance evaluation flow chart from the thin films deposition to the demonstrator

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